

# RankFilter: median, percentile and defect-pixel-correction IP

Streaming 3×3 to 7×7 rank filters for FPGA and ASIC video, at 1, 2 or 4 pixels per clock. Fewer comparators per pixel, with every network proved correct.

RankFilter is a family of streaming two-dimensional rank filters for camera and video pipelines. Each output pixel is the median, or a chosen percentile, of its K×K neighbourhood. A Bayer variant works on raw sensor data and can replace only the pixels that deviate from their same-colour neighbours, which is how hot and dead pixels are usually corrected.

The cores reuse work between overlapping windows. A 5×5 median needs 52 comparators per output pixel, where the best published single-window network needs 85. Every comparator network is proved correct in the Lean 4 proof assistant, and the cores have run on Intel Cyclone V silicon with zero mismatches against a reference model.

## 52

comparators per pixel for a 5×5 median (best single-window network: 85)

## −61 %

LUTs against Lattice's Median Filter IP at 7×7 (published figures, page 2)

## 4K60

at 4 pixels per clock on the slowest ECP5, Artix-7 and Cyclone V speed grades

## 0

mismatches in a continuous self-test on Cyclone V silicon, up to 170 MHz

## Features

- Median, 25th and 75th percentile; other ranks generated on request
- 3×3, 5×5 and 7×7 windows
- Defect-pixel correction for Bayer and monochrome sensors with a run-time threshold; the monochrome core also takes a static bad-pixel map
- 1, 2 or 4 pixels per clock (frame width a multiple of 2 or 4)
- AXI4-Stream video in and out with full back-pressure, or a smaller video-timing version for sensor streams that cannot stall
- Frame size set at run time; 2048-pixel lines by default, configurable
- Edge handling: replicate the border pixel, or use a constant
- Line buffers in block RAM, inferred or as ECP5 DP16KD primitives
- Pixel width is a parameter (verified at 8, 10, 12 and 16 bits)
- Credit-based flow control, formally proved never to drop or overwrite data
- Plain synthesisable Verilog-2005; no vendor-specific primitives required

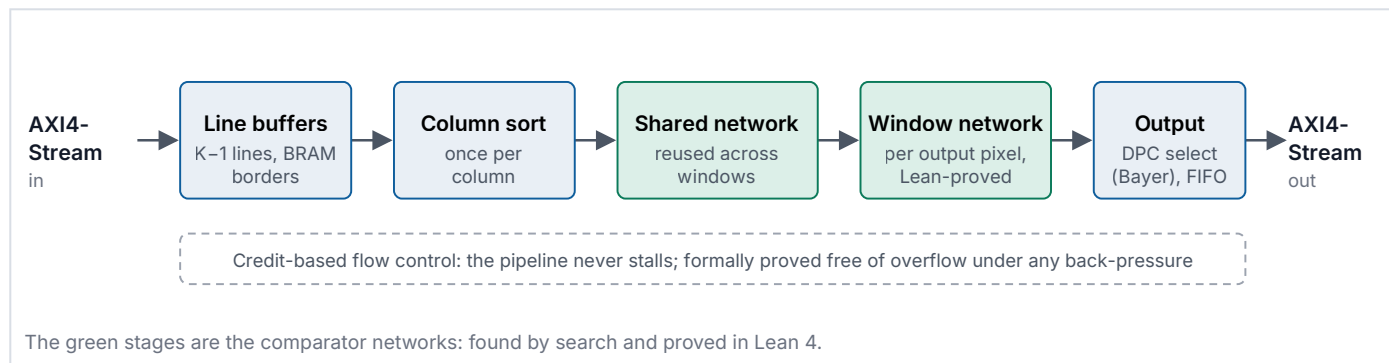
## Applications

- Hot and dead pixel correction on Bayer colour and monochrome sensors, including thermal and SWIR, from a threshold or a factory defect map
- Impulse (salt-and-pepper) noise removal
- Pre-processing for machine vision and industrial inspection
- Rank-order and grey-scale morphological filtering
- Scientific, medical and broadcast imaging

## Supported devices

Any FPGA or ASIC flow that accepts Verilog. Measured on Lattice ECP5, AMD Artix-7, Intel Cyclone V, SkyWater 130 nm and the ASAP7 7 nm research PDK.

## Block diagram



## Performance and size (complete filter: AXI4-Stream, line buffers, borders; 8-bit pixels)

| Variant                     | Lattice ECP5-85F, -6 |      | AMD Artix-7 35T, -1 |      | Intel Cyclone V E, C8 |      |
|-----------------------------|----------------------|------|---------------------|------|-----------------------|------|
|                             | LUT4 / FF / EBR      | Fmax | LUT / FF            | Fmax | ALM / M10K            | Fmax |
| 3×3 median                  | 928 / 691 / 2        | 154  | 861 / 773           | 203  | 371 / 7               | 180  |
| 3×3 median, 4 px/clock      | 2233 / 1783 / 8      | 164  | 1968 / 1752         | 183  | 939 / 8               | 180  |
| 5×5 median                  | 2056 / 1905 / 4      | 164  | 2105 / 1687         | 199  | 896 / 10              | 180  |
| 5×5 median, 4 px/clock      | 5184 / 6600 / 15     | 161  | 5354 / 3761         | 185  | 2216 / 28             | 164  |
| 5×5 25th percentile         | 1783 / 1622 / 4      | 170  | 1838 / 1476         | 194  | 769 / 10              | 180  |
| 7×7 median                  | 4455 / 4612 / 6      | 159  | 4613 / 3522         | 196  | 1941 / 20             | 171  |
| 7×7 median, 4 px/clock      | 11452 / 14490 / 23   | 143  | 12112 / 7438        | 156  | 5276 / 46             | 160  |
| Bayer DPC (same-colour 3×3) | 1092 / 1019 / 4      | 166  | 1060 / 986          | 181  | 435 / 9               | 164  |
| Bayer DPC, 4 px/clock       | 2673 / 2458 / 15     | 154  | 2593 / 2120         | 174  | 1115 / 11             | 180  |

Fmax in MHz. ECP5 and Artix-7: median of 5 placement seeds with open-source tools (yosys, nextpnr), not vendor sign-off. Cyclone V: Quartus Prime Lite TimeQuest, worst slow corner, median of 3 seeds (180 MHz is the device's clock-network limit here). 1080p60 needs 148.5 MHz at 1 pixel per clock; 4K60 needs 124.4 MHz at 4 pixels per clock; every 4-pixel variant meets it on every seed, at 8-bit and at 12-bit. 12-bit pixels add 22–47 % logic. The datasheet lists the other variants.

## Comparators per output pixel

5×5 median, one output pixel per clock

|                        |     |
|------------------------|-----|
| Odd-even transposition | 234 |
| Best single window     | 85  |
| Adams 2021             | 63  |
| RankFilter             | 52  |

| Window              | RankFilter | Adams 2021  | Single window |
|---------------------|------------|-------------|---------------|
| 5×5, 1 px/clock     | 52         | 63          | 85            |
| 5×5, 4 px/clock     | 37         | 42.75       | 85            |
| 7×7, 1 px/clock     | 140        | 187         | 231           |
| 7×7, 2 / 4 px/clock | 92         | 117 / 93.25 | 231           |
| 3×3, 1 px/clock     | 13         | 13          | 19            |

Odd-even transposition: the network HLS vision libraries unroll (234 after pruning). Single window: Dobbelaere's records. Adams 2021 (ACM TOG) is a software method; his 4-pixel figures are 2×2 output tiles, and 117 is our count of his method. At 3×3, 1 pixel per clock, the two tie.

## Verification

- Every comparator network is proved in Lean 4 to select the right rank for every input and any pixel type.
- The generated RTL is simulated on every binary window ( $2^{25}$  for 5×5; every sorted-column state for 7×7), which by the 0-1 principle covers all pixel widths.
- SymbiYosys proves the flow control never overflows, under any back-pressure, and follows the AXI4-Stream rules.
- Output on photographs is byte-identical to an independent Python reference model, under random back-pressure.
- On Intel Cyclone V silicon (Analogue Pocket), a continuous self-test of five variants, repeating a fixed test pattern under random back-pressure, found zero mismatches at 74 to 170 MHz.

## Against other cores

| Comparison                                                      | 5×5         | 7×7           |
|-----------------------------------------------------------------|-------------|---------------|
| Strongest baseline we built, same wrapper and tools (ECP5 LUT4) | -11 %       | -21 %         |
| Same, Cyclone V ALMs (Quartus)                                  | -18 %       | -22 %         |
| Lattice Median Filter IP, published LatticeECP3 LUTs            | 2908 → 2056 | 11,536 → 4455 |
| ASIC area / power, sky130 at 200 MHz (cores)                    | -16 / -18 % | -25 / -39 %   |

Strongest baseline: shared column sorting with the best selection stage we found, through the same wrapper and tools. Lattice figures come from its product page (IP v1.0, Diamond and Synplify): another family and toolchain, shown for scale. At 3×3 Lattice's core is smaller (680 LUTs against 928) because our AXI4-Stream wrapper dominates. ASIC results are from open PDKs.

## Deliverables

- Verilog source for each variant: an FPGA set and an ASIC-tuned set
- Datasheet with interface, timing and integration notes
- Bit-exact Python reference model and golden test vectors
- Self-checking SystemVerilog testbench
- Board self-test with expected checksum
- The Lean proof files

**Evaluation and licensing:** A simulation evaluation package is available on request. Source-code licences per project or per company. Custom variants (window size, rank, pixel width, pixels per clock) can be generated and verified to order.

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